IN THE CLAIMS:

Please revise the claims as follows:

1. (Currently Amended) A method of manufacturing a semiconductor memory device capable of electrically writing and erasing data, said semiconductor memory device having a plurality of cell transistors for storing data, each of said cell transistors having a floating gate electrode and a control gate electrode, and a plurality of select transistors for controlling and selecting said cell transistors, said method comprising:

forming a channel region for each said cell transistor and for each said select transistor by forming source regions and drain regions in a substrate by ion implantation;

before forming the control gate electrodes of said cell transistors, exposing a surface of a said substrate directly above said channel regions of said select transistors fabricated in the same process as the cell transistors but not exposing a surface of a substrate directly above said channel regions of said cell transistors;

forming gate insulating films of said select transistors on the exposed surface of the substrate; and

forming the control gate electrodes of said cell transistors and forming gate electrodes of said select transistors on said gate insulating films.

2. (Previously Amended) The method of manufacturing a semiconductor memory device according to claim 1, further comprising:

simultaneously forming a first diffused layer serving as source and drain regions of said cell transistors and a second diffused layer serving as source and drain regions of said select transistors.

3. (Previously Amended) The method of manufacturing a semiconductor memory device according to claim 1, further comprising:

forming gate insulating films of transistors of a peripheral circuit comprising a logic operation circuit, simultaneously with the gate insulating films of said select transistors; and

forming gate electrodes of the transistors of said peripheral circuit simultaneously with the gate electrodes of said select transistors.

4. (Previously Amended) The method of manufacturing a semiconductor memory device according to claim 2, further comprising:

forming gate insulating films of transistors of a peripheral circuit comprising a logic operation circuit, simultaneously with the gate insulating films of said select transistors; and

forming gate electrodes of the transistors of said peripheral circuit simultaneously with the gate electrodes of said select transistors.

5. (Original Claim) The method of manufacturing a semiconductor memory device according to claim 3, wherein the gate insulating films of said select transistors have a film thickness which is the same as the film thickness of the gate insulating film of a transistor which requires a high withstand voltage, among the transistors of said peripheral circuit.

6. (Original Claim) The method of manufacturing a semiconductor memory device according to claim 4, wherein the gate insulating films of said select transistors have a film

thickness which is the same as the film thickness of the gate insulating film of a transistor which requires a high withstand voltage, among the transistors of said peripheral circuit.

7-12. (Previously Canceled)

13. (Previously Added) The method of manufacturing a semiconductor memory device according to claim 1, wherein said control gate comprises polysilicon.

14. (Previously Added) A method of manufacturing a semiconductor memory device, said method comprising:

forming a first oxide film on a wafer on a first area to contain a plurality of cells transistors in a flash EEPROM (electrically erasable programmable read only memory) and in a second area to contain select transistors, said first oxide film to become a tunneling oxide film for said cells;

forming successively, on said first oxide film in said first area and said second area, a second layer to become a floating gate for said cells, a pad oxide layer as a third layer for said cells, and a fourth layer to serve as a mask material;

etching said second layer, said third layer, and said fourth layer to form ion implant masks for said cell transistors and said select transistors;

forming source and drain diffusion regions for said cell transistors and said select transistors, using said ion implant masks and an ion implant process;

completing a gate structure for said cell transistors; and

in a channel region for each said select transistor, stripping off all layers including said first oxide film to expose said channel region.

15. (Previously Added) The method of claim 14, further comprising:

completing a gate structure for each said select transistor above its corresponding channel region.

16. (Previously Added) The method of claim 15, wherein a third area contains transistors of a peripheral circuit and said first oxide film and said second, third, and fourth layers are formed in said third area, and said stripping exposes regions in said third area to be a channel region, a source diffusion region, and a drain diffusion region for each said peripheral circuit transistor.

17. (Previously Added) The method of claim 16, wherein a gate structure for each said peripheral circuit transistor is formed simultaneously to said gate structure for each said select transistor, said method further comprising:

using said peripheral circuit transistor gate structures as an ion implant mask to form said source diffusion regions and said drain diffusion regions of said peripheral circuit transistors.

18. (Previously Added) The method of claim 16, wherein said peripheral circuit transistors comprise at least two types of transistors based on a withstand-voltage characteristic, and gate oxide layers of said at least two types of transistors are formed in a multi-oxidation process, thereby forming gate oxide layers of different thicknesses for each said at least two types of transistors.

19. (Previously Added) A method of manufacturing a flash EEPROM (electrically erasable programmable read only memory) having cell transistors and select transistors, each said cell transistor and each said select transistor to include a source diffusion region, a drain diffusion region, and a channel region therebetween, said method comprising:

simultaneously forming source diffusion regions, drain diffusion regions, and channel regions for said cell transistors and said select transistors;

successively providing a plurality of layers that allow gate structures to be formed between said source diffusion regions and said drain diffusion regions for said cell transistors, said plurality of layers being additionally provided in regions to contain said select transistor;

and stripping, in regions between said source diffusion regions and said drain diffusion regions of said select transistors, all layers of said plurality of layers to thereby expose channel regions of said select transistors.

20. (Previously Added) The method of claim 19, further comprising:

completing gate structures for said select transistors over said exposed channel regions of said select transistors.

21. (Previously Added) The method of claim 20, said flash EEPROM additionally including a plurality of transistors in a peripheral circuit, each said peripheral circuit transistor to include a source diffusion region, a drain diffusion region, and a channel therebetween,

wherein said stripping all layers to expose channel regions of said select transistors additionally strips all layers to expose source diffusion regions, drain diffusion regions,

and channels of said peripheral circuit transistors.

22. (Previously Added) The method of claim 21, wherein gate structures of said peripheral circuit transistors are completed simultaneously with said gate structures of said select transistors.

23. (Previously Added) The method of claim 22, further comprising:

forming source diffusion regions and drain diffusion regions for said peripheral circuit transistors with an ion implant process, using said gate structures of said peripheral circuit transistors as an ion implant mask.

24. (Previously Added) The method of claim 21, wherein said peripheral circuit transistors comprise at least two types of transistors based on a withstand-voltage characteristic, and gate oxide layers of said at least two types of transistors are formed in a multi-oxidation process, thereby forming gate oxide layers of different thicknesses for each said at least two types of transistors.